

ELECTRICAL ENGINEERING (Paper I)

Time Allowed : Three Hours

Maximum Marks : 300

QUESTION PAPER SPECIFIC INSTRUCTIONS

(Please read each of the following instructions carefully before attempting questions)

There are EIGHT questions divided in two Sections.

Candidate has to attempt FIVE questions in all.

Question Nos. 1 and 5 are compulsory and out of the remaining, any THREE are to be attempted choosing at least ONE question from each Section.

The number of marks carried by a question/part is indicated against it.

Wherever any assumptions are made for answering a question, they must be clearly indicated.

Word limit in questions, wherever specified, should be adhered to.

SECTION 'A'

1. Answer any three of the following:
 - (a) The h-parameters of a 2-port network used in the circuit of Fig. 1a are $h_{11}=100\ \Omega$, $h_{12}=0.0025$, $h_{21}=20$ and $h_{22}=1\ \text{mS}$. Find the ratio V_2/V_1 .
[Figure: Fig. 1a: Source V_s (+ at top) in series with a $1\ \text{k}\Omega$ resistor feeding input port 1 of a box marked "2-PORT NETWORK"; input voltage V_1 across port 1 (+ at top); output port 2 (voltage V_2 , + at top) loaded by $R_L=2\ \text{k}\Omega$] 20
 - (b) A hollow cylindrical conductor of length L and radius R and carrying a surface current of density $J_b = J_z \hat{z}$ A/m is placed in a B-field given by $B = a/r \hat{r} + b \hat{\phi}$ T. Find the magnitude and direction of torque on the conductor. 20
 - (c) Using Thevenin's theorem, determine the current in the $2\ \Omega$ resistor in the circuit of Fig. 1c.
[Figure: Fig. 1c: Four parallel branches between a top line and a bottom (common) line. Branch 1 (left): voltage source $24\ \text{V}$ (?) (+ at top) in series with an $8\ \Omega$ (?) resistor in the top line, the resistor joining the source to the top line node of branch 2. Branch 2: current source $2\ \text{A}$ (arrow upwards) in parallel with a $20\ \Omega$ resistor, connected between the top and bottom lines. Branch 3: $10\ \Omega$ resistor in series with a battery of $36\ \text{V}$ (?) (label blurred; plate polarity not legible), from the top line to the bottom line. Branch 4 (right): $2\ \Omega$ resistor between terminals A (top) and B (bottom), connected across the top and bottom lines] 20
 - (d)(i) Give the schematic of two synchro pairs, one pair being useful for remote control and the other pair functioning as a transducer for converting angular position into an electrical signal. 10
 - (d)(ii) Give a typical set up for measuring the strain of a cantilever beam, with temperature compensation. 10
2. (a) A series R-L circuit with $R=50\ \Omega$ and $L=0.2\ \text{H}$ has a sinusoidal voltage $v(t)=75\sin(500t+0.785)$ applied at $t=0$, t being taken in sec. Find the complete current for $t>0$. What is the current at $t=0^+$? Why? 20
- (b) Show that an n -mesh, passive, three-terminal network may be replaced by a delta-connection of three impedances. Here n can be arbitrarily large. 20
- (c) A $300\ \text{kW}$, 0.65 lagging power factor load is shunted by a capacitor so that the power factor improves to 0.90 lagging. Find the kVAr that the capacitor must furnish and the reduction in apparent power. 20
3. (a) An aeroplane flies over the surface of the ocean and sends a $1\ \text{MHz}$ plane wave vertically downwards with a field intensity of $1000\ \text{V/m}$ just at the ocean surface. If a submarine requires a $10\ \mu\text{V/m}$ field, how deep can it be submerged and still be contacted by the aeroplane. The ocean water constants are $\sigma=4\ \text{S/m}$, $\mu_r=1$ and $\epsilon_r=81$. 20

- (b) A $2\text{ }\mu\text{C}$ charge is located at (0, 3, 0) m and a $4\text{ }\mu\text{C}$ charge at (4, 0, 0) m. Find the electric field at (0, 0, 5) m due to both these charges. 20
- (c) The phase velocity v_p of a wave of frequency f and wavelength λ is given by $v_p = c(\lambda_0/\lambda)^2$ where c and λ_0 are constants. Derive an expression for the group velocity v_g in terms of v_p and v_p . 20
4. (a) Using an RTD with $0.00251/^\circ\text{C}$ coefficient and $R(25^\circ\text{C})$ as $1000\text{ }\Omega$, design a Wheatstone bridge with an OP-AMP arrangement to provide a 0 to 10 V signal for a temperature span of 25°C to 125°C . 20
- (b)(i) Define the terms 'Dynamic error' and 'Resolution' of an instrument. Explain how these can be determined in the laboratory. 10
- (b)(ii) Give two examples each of active and passive transducers. Suggest suitable signal conditioning circuits for the same. 10
- (c) For the R-2R type of digital-to-analog converter shown in Fig. 4c, find the output voltage when S_4 is closed and S_3, S_2 and S_1 are grounded. 20
 [Figure: Fig. 4c: R-2R ladder DAC. Reference battery $V_B = 15\text{ V}$ (+ at top) between a top reference line and ground. Ladder line along the bottom: from ground a $2R$ resistor to node P, R from P to Q, R from Q to S, R from S to T. Four $2R$ legs hang from nodes P, Q, S and T respectively; the upper end of each leg goes to a changeover switch (S_4 for P, S_3 for Q, S_2 for S, S_1 for T) that connects it either to the top reference line (V_B) or to ground. Node T feeds the non-inverting input of an op-amp connected as a voltage follower (output joined to the inverting input); output v_o]
- SECTION 'B'**
5. Answer any three of the following:
- (a) In the circuit of Fig. 5a, the diode is ideal, $R=1.2\text{ k}\Omega$ and $I=5\text{ mA}$. Draw the $v - i$ characteristics of the circuit (i) with S open and $-10\text{ volt} < v < 15\text{ volt}$ and (ii) with S closed and $0 < v < 15\text{ volt}$ What happens when $v < 0$ with S closed? 20
 [Figure: Fig. 5a: Four branches in parallel between a top line and a bottom line: (1) voltage source v (+ at top), with current i marked in the top line leaving its + terminal; (2) switch S in series with an ideal diode, cathode towards S (top) and anode at the bottom line; (3) resistor R ; (4) current source I (arrow upwards)]
- (b) Show that the NMOS circuit of Fig. 5b is a NAND gate for positive logic. Write down the various combinations of inputs and output in a tabular form and clearly state the meanings of any symbols or parameters used therein. 20
 [Figure: Fig. 5b: Two n-channel MOSFETs Q_2 (upper, gate input v_2) and Q_1 (lower, gate input v_1) in series between the output node and ground; load MOSFET Q_3 (drawn horizontally, gate lead drawn upwards) between the output node and $+V_{DD}$; output v_o taken from the node joining Q_3 and the drain of Q_2]
- (c) Describe different methods for starting of synchronous motors. 20
- (d)(i) Explain the following terms as referred to an operational amplifier: (a) Input offset voltage and (b) Input offset current 10
- (d)(ii) The input $v_i(t)$ in the circuit of Fig. 5d is $v_i(t)=1.5\sin 2\pi \times 10^3 t$ volt with t in sec, Sketch $v_o(t)$ and label important points. 10
 [Figure: Fig. 5d: Op-amp; source $v_i(t)$ connected between the upper input terminal of the op-amp and ground; the lower input terminal is connected to ground through a $1\text{ k}\Omega$ resistor and to the output through a $3\text{ k}\Omega$ resistor; output $v_o(t)$ taken with respect to ground (input polarity marks on the op-amp not legible; the arrangement is a regenerative comparator)]
6. (a) Two single-phase transformers T_1 and T_2 , rated at 300 kVA and 400 WA respectively, when operated in parallel share a 500 WA , 0.8 lagging power factor as follows: T_1 : $192 + j 117\text{ kVA}$ T_2 : $210 + j 184\text{ kVA}$ Find the regulation of T_2 for rated kVA output at 0.8 lagging power factor when the percentage impedance of T_1 is $1.5 + j 6$. Also find the total load that the two transformers can share without any of these getting overloaded at 0.9 lagging p.f. 20
- (b) Two shunt generators rated at 150 kW and 250 kW when running at rated speeds have rated open circuit voltages of 245 V and 243 V respectively. Their external characteristics 20

are linear. The regulation of the 150 kW machine is 5% and that of the 250 kW machine is 4%, both in terms of their full Load terminal voltages, If these machines are connected in parallel, how much load will be carried by each machine when supplying a connected load of 360 kW? What will be the common terminal voltage?

- (c)(i) Name different types of single phase induction motors. Draw a comparison of their performance features. 5
- (c)(ii) ‘The range of stable operation of a three-phase induction motor can be extended by connecting a larger resistance in the rotor.’ Justify the statement. 5
- (c)(iii) Show that the reactive power drawn by a three-phase induction motor is maximum at standstill and decreases as the slip increases, the motor being operated at constant voltage. 10
7. (a) A 6-pole, 400 V, 50 Hz, 3-phase induction motor has a rotor resistance such that the maximum torque occurs at a slip of 0.2. An additional resistance of 0.5Ω has to be inserted to obtain 75% of the maximum torque at starting. Find the rotor resistance and reactance. 20
- (b) A 6600 V, 3-phase star-connected alternator has a resistance of 0.4Ω and a synchronous reactance of 6.0Ω per phase. If the regulation at full load 0.8 power factors leading is 7.5%, find the kVA rating of the alternator. 20
- (c)(i) What do you understand by the terms ‘short-circuit ratio and ‘synchronizing torque’ as applied to a synchronous generator? 10
- (c)(ii) A 1500 kVA, 4-pole, 3-phase, 50 Hz non-salient pole synchronous motor of negligible armature resistance having a synchronous reactance of 45Ω is operating on an infinite bus with its voltage at 6.6 kV 50 Hz. Find the synchronising torque per mechanical degree of rotor displacement (a) at no load and (b) when the motor is operating at full load with 0.85 leading power factor. 10
8. (a) Find the relation between v_o and v_s for the circuit of Fig. 8a and show that, with proper adjustments, the voltage v_o can be made proportional to the logarithm of the input voltage v_s .
[Figure: Fig. 8a: Input v_s (+) applied through a resistor to the inverting input of op-amp A_1 , whose non-inverting input is grounded; transistor Q_1 (base grounded) in the feedback path of A_1 , its collector joined to the inverting input and its emitter joined (dashed line) to the node after resistor R, which is in series with the output of A_1 ; this node also goes to the emitter of transistor Q_2 ; the collector of Q_2 is connected through R_2 [?] to V_R and, together with the base lead of Q_2 [?], to the non-inverting (+) input of op-amp A_2 ; A_2 is a non-inverting amplifier with R_4 from its output to its inverting input and R_3 from the inverting input to ground; output v_o (wiring around Q_2 partly unclear in the source)] 20
- (b) Find the mid-frequency gain of the amplifier shown in Fig. 8b. Neglect the loading effect of R_1 and R_2 . The transistor parameters with usual notations are $g_m=0.015$ S, $r_{b'e}=1 \Omega$, $r_{bb'}=90 \Omega$, $C_{b'e}=20$ pF and $C_{b'e}=3$ pF while $R_E=1$ k Ω .
[Figure: Fig. 8b: Emitter follower: input source “IN” coupled through capacitor C_1 to the base of an npn transistor; bias divider R_1 from V_{CC} to the base and a lower resistor (printed R_5 , i.e. R_2 [?]) from the base to ground; collector connected directly to V_{CC} ; emitter resistor R_E from the emitter to ground; output “OUT” taken from the emitter through a coupling capacitor, with respect to ground] 20
- (c) Design a combinational logic circuit to generate the 2’s complement of a 2-bit number. You may use two full adders and other gates as required but keeping the number of other gates to a minimum. 20