

ELECTRICAL ENGINEERING (Paper I)

Time Allowed : Three Hours

Maximum Marks : 300

QUESTION PAPER SPECIFIC INSTRUCTIONS

(Please read each of the following instructions carefully before attempting questions)

There are EIGHT questions divided in two Sections.

Candidate has to attempt FIVE questions in all.

Question Nos. 1 and 5 are compulsory and out of the remaining, any THREE are to be attempted choosing at least ONE question from each Section.

All questions carry equal marks.

Wherever any assumptions are made for answering a question, they must be clearly indicated.

Word limit in questions, wherever specified, should be adhered to.

SECTION 'A'

1. Answer any three of the following
 - (a) Consider the electric field due to an infinitely long uniform line charge. Show that the divergence of this field is zero.
 - (b) Fig. Q. 1(b) shows the details of a portion of a d.c. network. Evaluate the voltage V .
 [Figure: Fig. Q 1(b): Two networks N_1 (top) and N_2 (bottom) joined by two vertical wires: in the left wire a current of 3 A flows downwards (from N_1 to N_2), in the right wire a current of 2 A flows upwards (from N_2 to N_1). A third terminal of N_1 is connected by the top line to the top corner of a bridge, and a third terminal of N_2 by the bottom line to the bottom corner of the bridge; the voltage between the top and bottom lines is marked V_x [?] (+ at the top line). Bridge (diamond) arms: top corner to left corner 1 Ω ; top corner to right corner 3 Ω ; left corner to bottom corner 1 Ω ; right corner to bottom corner 1 Ω [?]; between the left and right corners a 1 Ω [?] resistor in series with a 4 V battery (polarity not legible)]
 - (c) In the a.c. circuit of Fig. Q.1(c), the rms values of different voltages under steady state are: $V_S = 16$ V; $V_R = 10$ V; $V_1 = 10$ V; $V_2 = 7$ V. Find the value of R_L .
 [Figure: Fig. Q 1(c): A.c. source V_S in series with resistor $R = 16$ Ω (voltage V_R across it) feeding the input port (voltage V_1) of a box marked "LC 2-port network"; the output port (voltage V_2) is loaded by resistor R_L]
 - (d) Justify the following statements: (i) It is advisable to measure a small quantity directly and not to deduce it as the difference of two individually measured large values. (ii) The plain Wheatstone bridge method is not suitable measurement of low-valued resistors.
2. (a) Find the rms value of current through the switch S when it is closed in the 3-phase circuit shown in Fig. Q. 2(a). Hence find the rms value of voltage across it when S is opened.
 $Z_1 = 40 + j0$ ohms, $Z_2 = j80$ ohms
 [Figure: Fig. Q 2(a): 3-phase balanced 400 V supply with three line terminals; a star-connected load with impedance Z_1 in each of the three phases; in the first line, impedance Z_2 is connected in series between the supply terminal and the Z_1 of that phase, and switch S is connected across (in parallel with) Z_2 ; the other two lines go directly to their Z_1 arms]
- (b) The two figures show a linear reciprocal 2-port network N under two different terminal conditions. The switches are closed at $t=0$ in both the circuits with zero initial conditions in N. Given that the currents in (i) for $t>0$ are: $i_1 = 0.5(e^{-t} + e^{-3t})$ amps; $i_2 = 0.1(3e^{-3t} - e^{-t})$ amps, find $v_1(t)$ for $t>0$ in (ii).
 [Figure: Fig. Q2(b): (i) A 1 V battery connected through a switch (closed at $t = 0$) to port 1 (terminals 1–1') of network N, input current i_1 entering terminal 1; port 2 (terminals 2–2') short-circuited, with current i_2 in the short (arrow downwards from 2' towards 2'). (ii) Port 1 (1–1') open-circuited, voltage v_1 across it (+ at terminal 1); a 2 V battery connected through a switch (closed at $t = 0$) across port 2 (2–2')]
- (c) A digital filter is characterised by the following recursive relation, where $x(n)$ and $y(n)$ are the input and output samples at the n^{th} sampling instant. The sampling frequency is 100 Hz. $y(n) = 0.8y(n-1) - 0.64y(n-2) + x(n) - x(n-1) + x(n-2)$ Find the poles and zeros of the

discrete-time transfer function of the filter. Hence deduce and sketch the magnitude response characteristic of the filter from $f=0$ to $f=\infty$. Mark the values at $f=0$, 50 and 100 Hz.

3. (a) Consider an electric displacement vector $\mathbf{D}=15\exp((-r)/x_0)\hat{r}-z/x_0\hat{z}$ c/m² in cylindrical coordinates r, ϕ, z . Calculate the outward flux crossing a right circular cylinder of radius $2x_0$, its axis coinciding with the z -axis and with the two plane faces at $z=0$ and $z=5x_0$, where $x_0=1$ cm.
- (b) Derive an expression for the inductance per unit length of a coaxial cable with radii a and b . Also calculate the value when $a=0.5$ cm and $b=2.0$ cm.
- (c) A 2 m long current carrying conductor is aligned in y -direction, its x -and z -coordinates being 5 m each. The current is 8 A in the negative y -direction. The conductor is subjected to a uniform magnetic field and the resulting force on the conductor is $4\times 10^{-3}(-\hat{i}_x+\hat{i}_z)$ N. Find the magnetic flux density (of the applied field).
4. (a) A 20 k Ω standard resistor R_s and a test resistor R_x are connected in series across a d.c. voltage source of negligible internal resistance. The voltages across R_s , R_x and the source are measured in turn by an accurate 0 – 120 V d.c. voltmeter. The readings obtained are 75 V, 21 V and 100 V respectively. Find the sensitivity of the d.c. voltmeter.
- (b) Give the block diagram of a typical modern digital counter and show how it is used to measure the frequency of a given test signal. What other categories of measurement can be performed using a digital counter?
- (c) A thermo-electric sensor with a time constant of 50 ms is used to record the temperature of a furnace. Assuming that the furnace temperature varies sinusoidally between the two limits 300°C and 500°C with a frequency of 2 Hz, determine the limits of the temperature as recorded from the sensor. Indicate a method of reducing the resultant error.

SECTION 'B'

5. Answer any three of the following:
 - (a) Explain how the input current changes in a three phase synchronous motor with constant load when the field current is varied. Draw phasor diagrams.
 - (b) In the circuit of Fig. Q 5(b), the diodes are ideal. Determine and sketch $v_0(t)$ for $0 < t < 8$ ms when $v_1(t)$ is a square waveform of ± 1 V amplitude, 8 ms period with a positive going zero crossing at $t=0$, the input $v_2(t)$ $2 \sin \pi t/3$ volt with t in ms and $v_3(t)$ is a 3 V amplitude rectangular pulse existing over $1 \text{ ms} < t < 3 \text{ ms}$.
 [Figure: Fig. Q 5(b): Three inputs $v_1(t)$, $v_2(t)$ and $v_3(t)$, each connected to the anode of an ideal diode; the three cathodes are joined to a common node, which is connected to ground through resistor R ; output $v_0(t)$ taken from the common node]
 - (c) Calculate the conductivity of silicon when it is doped by an n-type impurity to the extent of 1 in 10^6 . The atomic density of silicon is 5×10^{22} atoms/cm³, the intrinsic carrier density is 1.48×10^{10} pair/cm³ and the mobilities are 500 cm²/V-s and 1300 cm²/V-s. Compare the conductivity with that of intrinsic silicon.
 - (d) The circuit shown in Fig. Q. 5(d) is using master-slave flip-flops. V_{CC} is high and can be taken to be 1. Find B_0 and B_1 for the first seven clock cycles after these are initially cleared. Give precise explanations for your answers.
 [Figure: Fig. Q.5(d): Two JK master-slave flip-flops. FF1: inputs J_1 and K_1 tied together to V_{CC} ; clock input C_1 driven by CLK; output Q_1 gives B_0 and also drives the clock input C_2 of FF2. FF2: inputs J_2 and K_2 tied together to terminal A (note: "A is at V_{CC} "); output Q_2 gives B_1 . The clear ($\overline{CR}$) inputs of both flip-flops are joined and taken through a switch to V_{CC}]
6. (a) Two & [?] series motors with different airgaps, but otherwise identical, run at 700 and 750 rpm respectively, when taking 50 A at 500 V. The resistance of each motor including the series field is 0.36 Ω . If the two motors are mechanically coupled and connected in series to 500 V supply taking a current of 50 A, determine the speed and the voltage across each

machine.

- (b) Two single phase transformers, T_1 and T_2 are operated in parallel on both sides. The transformer, T_1 is rated at 100 kVA having a percentage impedance of $(1 + j5)$, The transformer, T_2 is rated at 200 kVA having a percentage impedance of $(1.5 + j4)$. Calculate the load shared by each, when the total load is 250 kVA at 0.8 power factor lagging. Also calculate the total load at the same power factor that the two transformers in parallel can supply such that neither of the transformers gets overloaded.
 - (c) Explain the following in relation to a plain single phase induction motor: (i) It fails to start when connected to ac supply. (ii) If it is started in either direction, it continues to rotate in the same direction.
7. (a) A 3-phase, 6600 V, 100 kVA, synchronous generator delivers rated current at 0.8 pf lagging, the load voltage being 6 kV. The resistance and synchronous reactance per phase are 1Ω and 30Ω respectively. Calculate the load voltage when the load current remains same at rated value, but the power factor changes to 0.8 leading. The field current is the same as before.
- (b) The rotor of a 3-phase, 6-pole, 50 Hz, slip-ring induction motor has resistance of 0.2Ω per phase and runs at 960 rpm on full load. Calculate the resistance to be inserted in the rotor circuit so that the speed reduces to 800 rpm, with torque (i) remaining constant, and (ii) varying as square of speed. Neglect stator impedance. Make assumptions as needed.
- (c) A 400 V, 15 kW, dc shunt motor takes 42 A and runs at 1200 rpm. The resistances of armature and field are 0.8Ω and 200Ω respectively. Neglect armature reaction. (i) Find the field current required to reduce the speed to 1000 rpm with load torque at half of previous value. (ii) Find also the initial armature current, when the field current is changed to that found in (i), with the speed not changing instantaneously.
8. (a) Find the CB h-parameters of a transistor in terms of its r-parameters and α .
- (b) A silicon transistor has a β -independent bias using an emitter resistor potential divider combination. The emitter circuit resistance is 300Ω , the collector circuit resistance is 500Ω , collector supply voltage is 15 V and $\beta=100$. Find the potential divider resistances so that maximum symmetrical swing is permitted at the collector. Take $V_{CE,sat}=0$.
- (c) Describe a successive approximation type of an A to D converter and give its merits. Find the conversion time and the resolution of an 8-bit ADC of this type when the clock period is $1.25 \mu s$.